Amendment to the Claims:

The claims under examination in this application, including their current status and changes made in this paper, are respectfully presented.

1. A drain-extended transistor, formed at a semiconductor surface of a body, comprising:

a first source region of first conductivity type, and disposed at a region of the surface having a second conductivity type;

an insulating structure disposed at the surface near the first source region, and disposed over a portion of a lightly-doped region of the first conductivity type to define a drift region thereunder;

at least one drain region of the first conductivity type disposed in the lightly-doped region and spaced from the first source region by the first isolation structure;

a plurality of channel regions of the second conductivity type disposed adjacent the first source region in the region of the surface having the second conductivity type, and disposed between the first source region and the at least one drain region;

at least one isolation structure disposed between adjacent ones of the plurality of channel regions;

at least one doped region of the second conductivity type, each underlying a corresponding isolation structure; and

a gate electrode disposed over the plurality of channel regions, over the plurality of isolation structures, and over at least a portion of the drift region.

2. The transistor of claim 1, further comprising:

an insulator layer disposed over the first source region, the gate electrode, and the at least one drain region; and

a plurality of metal conductors, each in contact with a corresponding one of the first source region, gate electrode and the at least one drain region through contact openings in the insulator layer.

3. The transistor of claim 2, further comprising:

a backgate contact region, of the second conductivity type, disposed at the region of the surface having the second conductivity type near the source region; and

a metal conductor in contact with the backgate contact region through a contact opening in the insulator layer.

4. The transistor of claim 1, further comprising:

a backgate contact region, of the second conductivity type, disposed at the region of the surface having the second conductivity type near the source region.

5. The transistor of claim 1, wherein the at least one drain region comprises a plurality of drain regions, each associated with a corresponding one of the plurality of channel regions.

6. The transistor of claim 5, wherein the insulating structure is disposed between each of the plurality of drain regions and the corresponding ones of the plurality of channel regions.

7. The transistor of claim 6, further comprising:

a doped region of the first conductivity type underlying the insulating structure.

8. The transistor of claim 1, wherein the at least one doped region of the second conductivity type has a dopant concentration at least about one order of magnitude higher than that of the region of the surface having a second conductivity type.

9. The transistor of claim 1, wherein the lightly-doped region comprises a well region extending beyond the insulating region toward the source region, so that the at least one isolation structure overlaps the well region;

and further comprising:

at least one doped region of the first conductivity type, each underlying a portion of a corresponding isolation structure in the well region.

10. The transistor of claim 9, wherein the at least one doped region of the first conductivity type has a dopant concentration at least about one order of magnitude higher than that of the well region.

11. The transistor of claim 1, wherein the at least one doped region of the second conductivity type has a dopant concentration at least about one order of magnitude higher than that of the region of the surface having a second conductivity type.

12. The transistor of claim 11, wherein the region of the surface having a second conductivity type comprises a well of the second conductivity type disposed at a region of the surface.

13. The transistor of claim 1, wherein the region of the surface having a second conductivity type comprises a well of the second conductivity type disposed at a region of the surface.

14. The transistor of claim 1, wherein the first conductivity type is n-type and the second conductivity type is p-type.

15. The transistor of claim 1, wherein the insulating structure and the at least one isolation structure are contiguous with one another.

16. The transistor of claim 15, wherein the insulating structure and the at least one isolation structure each comprise field oxide.

17. The transistor of claim 15, wherein the insulating structure and the at least one isolation structure are each comprise a deposited insulator structure disposed within a trench in the surface.

18. A method of fabricating a drain-extended transistor, comprising:

forming a first lightly-doped region of a first conductivity type at a selected location of a semiconductor surface of a body;

forming a second lightly-doped region of a second conductivity type at a selected location of the semiconductor surface;

implanting dopant of the first conductivity type into selected locations of the first lightly-doped region;

forming isolation structures at the selected locations of the first lightly-doped region at which dopant of the first conductivity type is implanted in the implanting step, and an isolation structure at a selected location of the second lightly-doped region;

forming a gate electrode over the surface, the gate electrode overlapping portions of the isolation structures at selected locations of the first lightly-doped region, and overlapping a plurality of channel regions of the first lightly-doped region disposed between the isolation structures;

forming a source region at a selected location of the first lightly-doped region; and

forming at least one drain region at a selected location of the second lightly-doped region, the at least one drain region spaced apart from the plurality of channel regions by the isolation structure at the selected location of the second lightly-doped region.

19. The method of claim 18, wherein the step of forming the first lightly-doped region comprises:

forming a well region of the first conductivity type into a selected location of a semiconductor layer of the second conductivity type.

20. The method of claim 18, wherein the step of forming the second lightly-doped region comprises:

forming a well region of the second conductivity type into a selected location of a semiconductor layer of the first conductivity type.

21. The method of claim 18, further comprising:

implanting dopant of the second conductivity type into selected locations at the second lightly-doped region,;

wherein the step of forming isolation structures also forms isolation structures at one or more of the selected locations of the second lightly-doped region at which dopant of the first conductivity type is implanted in the implanting step.

22 (amended) ~~20~~. The method of claim 18, wherein the first conductivity type is p-type and the second conductivity type is n-type.

23 (amended) ~~21~~. The method of claim 18, wherein the step of forming at least one drain region forms a plurality of drain regions, each spaced apart from a corresponding one of the plurality of channel regions by the isolation structure at the selected location of the second lightly-doped region.

24 (amended) ~~22~~. The method of claim 18, further comprising:

forming a patterned nitride layer at the surface of the first lightly-doped region; and

oxidizing the locations of the surface exposed by the patterned nitride layer.

25 (amended) ~~24~~. The method of claim ~~22~~ 23, wherein the step of forming isolation structures comprises:

etching trenches into selected locations of the first lightly-doped region; and

depositing an insulating material into the trenches.